Features

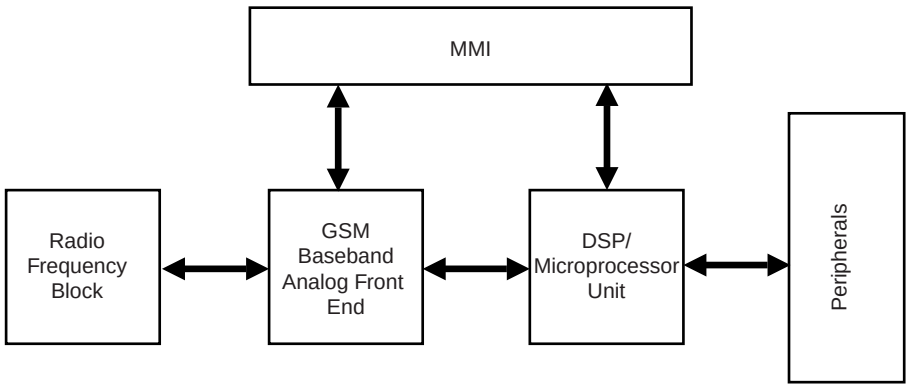
- **Voice Analog-to-Digital, Digital-to-Analog Interface Compliant with G.712 and GSM Requirements**
- **DTMF and Single Tone Generator**
- **Analog RF Interface (Transmit I/Q, Receive I/Q)**
- **Receive and Transmit Baseband Filtering which Meets the GSM System Requirements**
- **Interrupt Controller**
- **System Clock Generation**
- **Timing Generation and Control**
- **GMSK Modulation**
- **RF Control, including: AFC, AGC, Power Level, and Synthesizer Programming**
- **Signal Monitoring and Control via Auxiliary ADCs and DACs**
- **Interface with DSP and Microcontroller**

Description

The GSM Baseband Analog Front End (AT75C6100) is an integrated mixed signal chip that provides the essential functions for controlling and interfacing to the various parts of a GSM system. Its main function is to provide an interface between the RF subsystem and the digital signal processor or microprocessor unit.

The AT75C6100 integrates on a single chip functions such as: GSM timing generation, GSM system control functions, analog front end (or RF codec) functions, and the audio codec functions.

Figure 1. GSM System Block Diagram



GSM Baseband Analog Front End

AT75C6100

Preliminary

Rev. 1287A–07/99

Pin Configuration

Figure 2. AT75C6100 Pinout

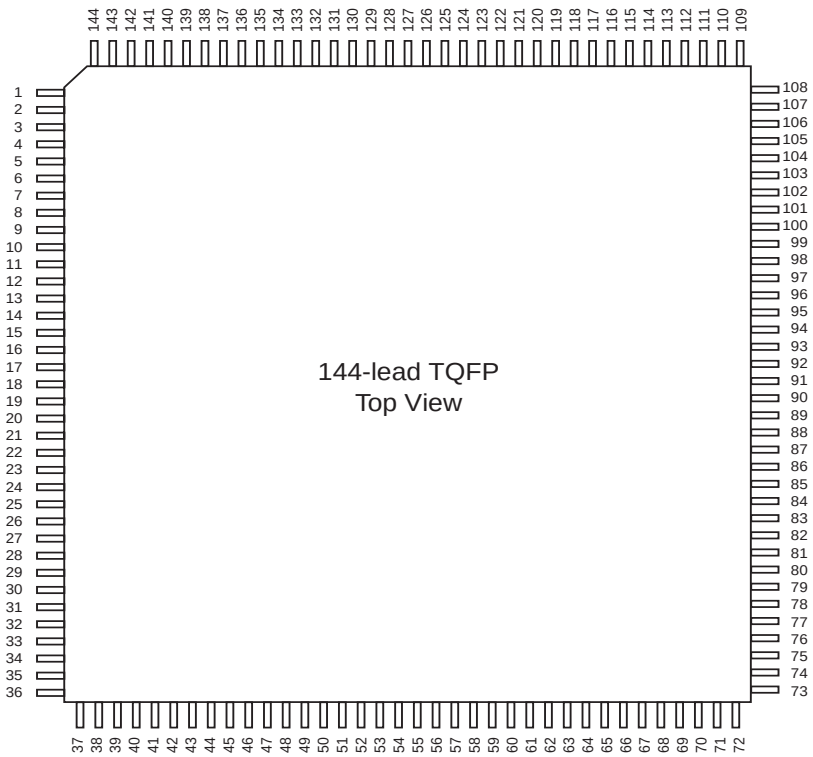


Table 1. Analog Pins

Pin	Signal	I/O	Description
28	auxoutn	O	Auxiliary Voice Codec Differential Output (Negative)
29	auxoutp	O	Auxiliary Voice Codec Differential Output (Positive)
30	earn	O	Earphone Differential Output (Negative)
31	earp	O	Earphone Differential Output (Positive)
34	vrefdec	O	Bandgap Reference Output
35	vcmdec	O	Unbuffered Common-mode Reference Output
36	vcm	O	Buffered Common-mode Reference Output
37	cout	O	Microphone Amplifier Offset Compensation Capacitor
38	micp	I	Microphone Differential Input (positive)
39	micn	I	Microphone Differential Input (negative)
40	auxinp	I	Auxiliary Differential Input (positive)
41	auxinn	I	Auxiliary Differential Input (negative)
45	outdac1	O	Automatic Frequency Control Output
48	outdac2	O	Automatic Gain Control Output

Table 1. Analog Pins (Continued)

Pin	Signal	I/O	Description
49	outdac3	O	PA Power Control Output
50	outdac4	O	Auxiliary Control Output
53	txqn	O	Differential Transmit Path Channel Q Output (Negative)
54	txqp	O	Differential Transmit Path Channel Q Output (Positive)
55	txip	O	Differential Transmit Path Channel I Output (Positive)
56	txin	O	Differential Transmit Path Channel I Output (Negative)
59	vcm_adc	O	Decoupling of Common Mode Voltage for Auxiliary ADC
60	vbg_iq	O	Decoupling of Reference Voltage for IQ DAC & ADC
61	vcm_iq	O	Decoupling of Common Mode Voltage for IQ DAC & ADC
64	rxqp	I	Differential Receive Path Channel Q Input (Positive)
65	rxqn	I	Differential Receive Path Channel Q Input (Negative)
66	rxin	I	Differential Receive Path Channel I Input (Negative)
67	rxip	I	Differential Receive Path Channel I Input (Positive)
68	inadc3	I	Auxiliary Input ADC Port 3
69	inadc2	I	Auxiliary Input ADC Port 2
70	inadc1	I	Auxiliary Input ADC Port 1
131	clki2	I	Analog Low Level Clock Squarer Input

Table 2. Digital Pins

Pin	Signal	I/O	Description
2	ddata0	I/O/Z	DSP Data Bus: Bit 0
3	ddata1	I/O/Z	DSP Data Bus: Bit 1
4	ddata2	I/O/Z	DSP Data Bus: Bit 2
5	ddata3	I/O/Z	DSP Data Bus: Bit 3
6	ddata4	I/O/Z	DSP Data Bus: Bit 4
8	ddata5	I/O/Z	DSP Data Bus: Bit 5
9	ddata6	I/O/Z	DSP Data Bus: Bit 6
11	ddata7	I/O/Z	DSP Data Bus: Bit 7
12	ddata8	I/O/Z	DSP Data Bus: Bit 8
13	ddata9	I/O/Z	DSP Data Bus: Bit 9
14	ddata10	I/O/Z	DSP Data Bus: Bit 10
15	ddata11	I/O/Z	DSP Data Bus: Bit 11
16	ddata12	I/O/Z	DSP Data Bus: Bit 12
19	ddata13	I/O/Z	DSP Data Bus: Bit 13
21	ddata14	I/O/Z	DSP Data Bus: Bit 14
22	ddata15	I/O/Z	DSP Data Bus: Bit 15
23	drw	I	DSP Read/Write Signal

Table 2. Digital Pins (Continued)

Pin	Signal	I/O	Description
24	dcs	I	DSP Interface Chip Select Signal
25	dack	I	DSP Acknowledge Signal
26	dint	O	DSP Interrupt Request Signal
74	test0	I	Test Mode Select: Bit 0
75	test1	I	Test Mode Select: Bit 1
76	test2	I	Test Mode Select: Bit 2
77	rstil	I	Master Reset (Active Low)
78	bbce	I	Master Clock Enable (Active High)
79	port0	O	General Output Control Pin: Bit 0
80	port1	O	General Output Control Pin: Bit 1
81	port2	O	General Output Control Pin: Bit 2
82	mint	O	Microcontroller Interrupt Request Signal
84	mack	I	Microcontroller Acknowledge Signal
87	mcs	I	Microcontroller Interface Chip Select Signal
88	mrw	I	Microcontroller Read/Write Signal
89	mdata0	I/O/Z	Microcontroller Data Bus: Bit 0
90	mdata1	I/O/Z	Microcontroller Data Bus: Bit 1
91	mdata2	I/O/Z	Microcontroller Data Bus: Bit 2
93	mdata3	I/O/Z	Microcontroller Data Bus: Bit 3
94	mdata4	I/O/Z	Microcontroller Data Bus: Bit 4
96	mdata5	I/O/Z	Microcontroller Data Bus: Bit 5
97	mdata6	I/O/Z	Microcontroller Data Bus: Bit 6
98	mdata7	I/O/Z	Microcontroller Data Bus: Bit 7
100	madd0	I	Microcontroller Address Bus: Bit 0
101	madd1	I	Microcontroller Address Bus: Bit 1
102	madd2	I	Microcontroller Address Bus: Bit 2
104	madd3	I	Microcontroller Address Bus: Bit 3
105	madd4	I	Microcontroller Address Bus: Bit 4
106	madd5	I	Microcontroller Address Bus: Bit 5
107	madd6	I	Microcontroller Address Bus: Bit 6
110	synol	I	Synthesizer Out-of-Lock Signal (active high)
111	sclk	O	Synthesizer Serial Data Clock
112	sdata	O	Synthesizer Serial Data Bit
113	sle0	O	Synthesizer 0 Serial Data Latch Enable
114	sle1	O	Synthesizer 1 Serial Data Latch Enable
116	sle2	O	Synthesizer 2 Serial Data Latch Enable

Table 2. Digital Pins (Continued)

Pin	Signal	I/O	Description
119	agcdac0	O	Digital AGC Output: Bit 0
120	agcdac1	O	Digital AGC Output: Bit 1
121	agcdac2	O	Digital AGC Output: Bit 2
122	agcdac3	O	Digital AGC Output: Bit 3
124	agcdac4	O	Digital AGC Output: Bit 4
125	tx_on	O	Power Enable (Active High) for the Transmit Signal Processing
127	rx_on	O	Power Enable (Active High) for the Receiver I/Q Demodulator
129	pa_on	O	Power enable (Active High) for the Transmit Power Amplifier
133	clki1	I	Clock Input CMOS (13 MHz/26 MHz)
134	clke	I	Enables the Power (Active Low) to the clki2 Input Pin
135	clko1	O	Clock Output (13 MHz)
137	sse	I	Small Signal Clock Input Enable. When high, clki2 is taken as the clock input.
138	clko2	O	Synchronized Clock Output (520 kHz)
139	dadd0	I	DSP Address Bus: Bit 0
141	dadd1	I	DSP Address Bus: Bit 1
142	dadd2	I	DSP Address Bus: Bit 2
143	dadd3	I	DSP Address Bus: Bit 3

Table 3. Analog Power and Ground Pins

Pin	Signal	I/O	Description
27	PAVDDPWR	AVDD	Analog Power for Voiceband Codec Output Amplifier
32	PAGNDPWR	AGND	Analog Ground for Voiceband Codec Output Amplifier
33	PAVDDVOICE	AVDD	Analog Power for Voiceband Codec
42	PAGNDVOICE	AGND	Analog Ground for Voiceband Codec
43	PAVDDAFC	AVDD	Analog Power for AFC DACs
44	RINGAGND	AGND	Analog Ground for Internal Guard Ring
46	PAGNDAFC	AGND	Analog Ground for AFC DACs
47	PAVDDDAC	AVDD	Analog Power for Auxiliary DACs
51	PAGNDDAC	AGND	Analog Ground for Auxiliary DACs
52	PAVDDIQDAC	AVDD	Analog Power for IQ DAC Cells
57	PAGNDIQDAC	AGND	Analog Power for IQ DAC Cells
58	PAVDDVREF	AVDD	Analog Power for IQ Codec Reference Generator
62	PAGNDVREF	AGND	Analog Ground for IQ Codec Reference Generator
63	PAVDDIQADC	AVDD	Analog Power for Core & Periphery ADC IQ & Aux Cells
71	RINGAVDD	AVDD	Analog Supply for Internal Guard Ring

Table 3. Analog Power and Ground Pins (Continued)

Pin	Signal	I/O	Description
72	PAGNDIQADC	AGND	Analog Ground for Core & Periphery ADC IQ & Aux Cells
130	PAGNDCLK	AGND	Analog Ground for Clock Squarer
132	PAVDDCLK	AVDD	Analog Power for Clock Squarer

Table 4. Digital Power and Ground Pins

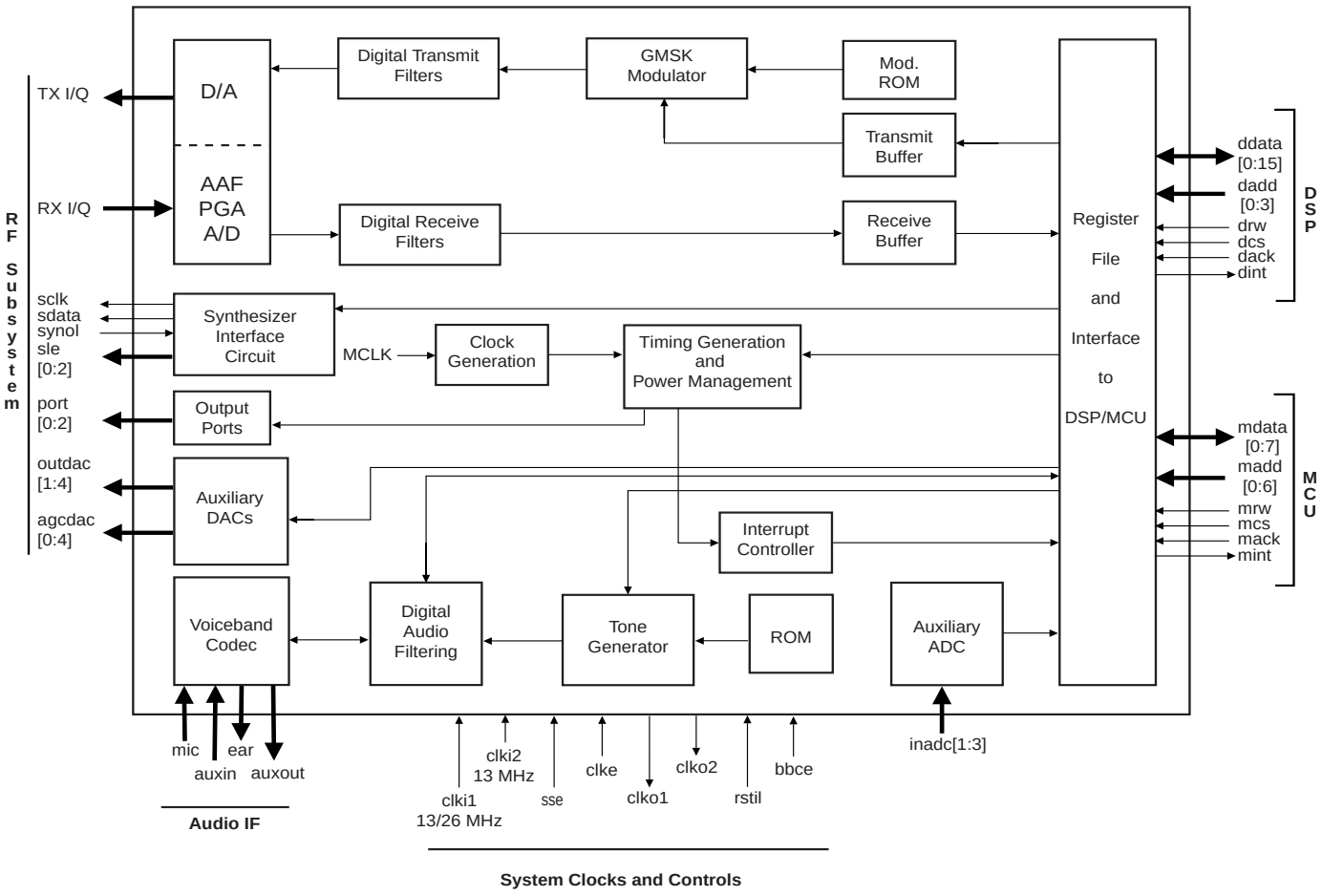
Pin	Signal	I/O	Description
1	VDDIVDD	DVDD	Digital Power: Internal (Core)
7	GNDVSSDC	DGND	Digital Ground: Shorted Internal (Core) & Quiet I/O (DC)
10	VDDVDDDC	DVDD	Digital Power: Shorted Internal (Core) & Quiet I/O (DC)
17	VSSAC	DGND	Digital Ground: Switching I/O (AC)
18	GNDVSSDC	DGND	Digital Ground: Shorted Internal (Core) & Quiet I/O (DC)
20	VDDVDDDC	DVDD	Digital Power: Shorted Internal (Core) & Quiet I/O (DC)
NC	VDDIVDD	DVDD	Digital Power: Internal (Core)
NC	VDDDC	DVDD	Digital Power: Quiet I/O (DC)
73	VDDAC	DVDD	Digital Power: Switching I/O (AC)
73	VDDAC	DVDD	Digital Power: Switching I/O (AC)
83	GNDVSSDC	DGND	Digital Ground: Shorted Internal (Core) & Quiet I/O (DC)
85	VSSAC	DGND	Digital Ground: Switching I/O (AC)
86	VDDVDDDC	DVDD	Digital Power: Shorted Internal (Core) & Quiet I/O (DC)
92	GNDVSSDC	DGND	Digital Ground: Shorted Internal (Core) & Quiet I/O (DC)
95	VDDVDDDC	DVDD	Digital Power: Shorted Internal (Core) & Quiet I/O (DC)
99	VDDAC	DVDD	Digital Power: Switching I/O (AC)
103	VDDVDDDC	DVDD	Digital Power: Shorted Internal (Core) & Quiet I/O (DC)
108	VSSAC	DGND	Digital Ground: Switching I/O (AC)
108	VSSAC	DGND	Digital Ground: Switching I/O (AC)
109	VSSDC	DGND	Digital Ground: Quiet I/O (DC)
109	GNDVSSI	DGND	Digital Ground: Internal (Core)
115	VDDAC	DVDD	Digital Power: Switching I/O (AC)
117	VDDVDDDC	DVDD	Digital Power: Shorted Internal (Core) & Quiet I/O (DC)
118	GNDVSSDC	DGND	Digital Ground: Shorted Internal (Core) & Quiet I/O (DC)
123	VDDVDDDC	DVDD	Digital Power: Shorted Internal (Core) & Quiet I/O (DC)
126	GNDVSSDC	DGND	Digital Ground: Shorted Internal (Core) & Quiet I/O (DC)
128	VSSAC	DGND	Digital Ground: Switching I/O (AC)
136	VSSAC	DGND	Digital Ground: Switching I/O (AC)

Table 4. Digital Power and Ground Pins (Continued)

Pin	Signal	I/O	Description
140	GNDVSSDC	DGND	Digital Ground: Shorted Internal (Core) & Quiet I/O (DC)
144	VDDAC	DVDD	Digital Power: Switching I/O (AC)
144	VDDAC	DVDD	Digital Power: Switching I/O (AC)

Block Diagram

Figure 3. Block Diagram of the GSM Baseband Analog Front End



Architectural Overview

The functional block diagram of the AT75C6100 is shown in Figure 3.

The AT75C6100, in conjunction with a digital signal processor or microprocessor unit, constitutes a 2-chip chipset solution for a GSM handheld mobile terminal. The AT75C6100 incorporates all the GSM timing generation circuitry from a master clock input of 13 MHz or 26 MHz. On one end, it interfaces to the RF subsystem and provides the analog-to-digital and digital-to-analog functions to digitize the analog I and Q signals coming from the RF on the receiver side, and to output the analog I and Q signals to the RF on the transmitter side. On the other end, it interfaces to the DSP through a set of control and data registers. On the receiver side, the AT75C6100 stores the I and Q samples in a double buffered FIFO to reduce the interrupt rate to the DSP. On the transmitter side, the AT75C6100 buffers the data bits to be transmitted, modulates, and generates the I and Q signals at the appropriate transmit slot.

The timing generation unit generates the timing signals for starting and ending the receive and transmit operations. The timing signals can be internal, for internal filters and buffers, or external, for RF and baseband control. The timing unit is controlled by a set of programmable registers that sequence the events in the frame.

The voice codec unit interfaces to a microphone and a speaker and contains the analog-to-digital, digital-to-analog, and the filtering operations that meet the G.712 and GSM audio specifications. The 16-bit PCM input and output audio words are accessed by the DSP through two 16-bit data registers. The voice codec module has a tone generator block that can generate up to two simultaneous tones.

The following is a list of the functional modules integrated on the AT75C6100 chip.

Radio Interface

Receive Section

- I and Q analog to digital data conversion from the baseband RF module, output to the DSP input.

The differential receive path contains the input programmable gain amplifiers, anti-aliasing filters, 3rd order sigma-delta analog-to-digital converters, and decimators. The digital I and Q output is placed in a double-buffered 64-location FIFO. Each of the 32 locations can contain up to 16 pairs of I/Q data. The DSP accesses the two halves alternately as a response of a AT75C6100-generated interrupt that indicates that 16 pairs are ready for reading.

Transmit Section

- GMSK modulation of the frame burst to quadrature I and Q, and digital-to-analog conversion to the baseband differential input of the RF module.

The transmitter section starts at the transmitter buffer which contains up to 160 data bits. The buffer is loaded by the DSP with the bits to be transmitted in the next transmission session. The transmitter module contains the GMSK modulator, interpolators, digital-to-analog converters, reconstruction filters, and output amplifiers.

Synthesizer Programming and Interface Circuitry

The synthesizer module is used to program the RF transmit, receive, and monitor frequencies. It interfaces directly with the most common synthesizers in the market and is programmable. Two modes of operation exist: manual programming and timed programming. In manual programming mode, the user needs to program the synthesizer many times during the frame (depending on the number of monitor slots used). In the timed programming mode, the user can load up to three different pieces of frequency information per frame with their desired time of synthesizer programming. The interface consists of a data line, a clock line and three latch enable lines.

Auxiliary Digital-to-Analog Converters

The AT75C6100 has four digital-to-analog converters for AFC (10-bit), AGC (10-bit), TX power control (10-bit), and auxiliary functions, e.g. LCD (8-bit). All the digital-to-analog converters operate at a 270.83 kHz sampling rate.

Auxiliary Analog-to-Digital Converter

The AT75C6100 has a 3-port analog-to-digital converter with 10 bits of resolution. The ADC can be shared for functions such as battery voltage and temperature measurement. The ADC operates at 27 kHz sampling rate.

Output Control Signals

The AT75C6100 contains a programmable set of three output signals for controlling external timed functions including the RF. They can be generated with an on/off timing precision of ±12/26 µs.

Timing and Power Management

Clock and Timing Generation

The AT75C6100 offers system clock generation including all the internal data sampling clocks, audio sampling clocks, and clock phase adjustment.

The device contains the clock generation module for the GSM system. All the clocks required internally for the filters and for timing generations are derived from the 13 MHz or

26 MHz master input clock. In addition, the user can adjust the sampling time of the I and Q analog-to-digital converters in steps of 12/13 µs.

The timing generation unit can be programmed to generate timing signals for the transmitter and receiver sessions. These signals include: the start timing, the length of the session, and any system-required path delays. In turn, this module generates any associated timing signals necessary to turn on or off internal clocks and RF sub-modules for power-saving purposes. The timing unit is clocked at the Q-bit rate of 13/12 MHz.

This unit also includes a programmable interrupt generator, which can be used to sequence the events in the GSM physical layer. These include all the interrupts for the internal AT75C6100 modules and external for the DSP and the microcontroller to initiate events in the corresponding device.

Voiceband Codec

Voiceband Analog-to-Digital Conversion from an External Microphone to the Input of the DSP

The voice codec section meets both the G.712 and GSM specifications. The output is a 16-bit PCM word at 8 kHz. The DSP accesses this data upon receiving an audio interrupt.

Voiceband Digital-to-Analog Conversion from the Output of the DSP to the External Speaker

The voice codec section meets both the G.712 and GSM specifications. The input is a 16-bit PCM word requested from the DSP by an 8 kHz interrupt.

DTMF and Call Progress Sidetone Generation

The AT75C6100 has a dual tone generator module that can produce a single or a dual tone in the range of 0 to 1990 Hz.

Parallel Interface to External Device

The AT75C6100 has two parallel interfaces to the external device; one for communication with the DSP and the other with the microcontroller. Communication is achieved through a set of memory-mapped registers for data, counters, and control. These registers are read or written by the external device. Eleven registers are memory-mapped to the DSP data space and 51 registers to the microcontroller data space. Table 5 defines these registers and their addresses.

The DSP memory-mapped registers can be accessed over a 16-bit data line. However, those mapped to the microcontroller memory space can only be accessed over an 8-bit data line. Hence, all microcontroller-mapped registers have two addresses; the even address accesses the low byte and the odd address accesses the high byte. On writing to a register of size greater than 8 bits, the write operation should be made successively, first low then high byte access. Only the AUXADC1/2/3 and INT_MASK_M registers need only one access to their even address (low byte). Reading the registers can be done in either order. On reading write-only registers, a value of zero is obtained. Unused bits are padded with zero when read.

Default values upon reset are indicated for certain registers (all of the START registers). If none is indicated, then the default is zero. The default values of control registers are indicated in the tables describing them.

Table 5. AT75C6100 Register Map

Name	Size	Addr	Function	R/W
Microcontroller Data Space Mapped Registers				
AUXDAC1	10	0, 1	Used for the AFC (also accessible by DSP)	W
AUXDAC2	10	2, 3	Used for the AGC (also accessible by DSP)	W
AUXDAC3	10	4, 5	Used for the power control to the RF	W
AUXDAC4	8	6, 7	Used for auxiliary control (e.g. LCD)	W
AUXADC1	10	8, 9	Used for aux ADC output port 1	R/W
AUXADC2	10	10, 11	Used for aux ADC output port 2	R/W
AUXADC3	10	12, 13	Used for aux ADC output port 3	R/W
SYNDATA0	16	14, 15	Synthesizer data word 0	W
SYNDATA1	16	16, 17	Synthesizer data word 1	W
SYNCTRL0	13	18, 19	Synthesizer control word 0	W
SYNCTRL1	10	20, 21	Synthesizer control word 1	W

Table 5. AT75C6100 Register Map (Continued)

Name	Size	Addr	Function	R/W
M_CONTROL1	11	22, 23	Control register accessed by the microcontroller.	R/W
RX_START	14	24, 25	The start of the receive slot. Default value: 0x3FFF.	W
RX_DEL	9	26, 27	Delay between RX_START and actual RX slot (size will depend on the HW delay). This time is used for power up and calibration delays. The 2 LSBs are always zero. Minimum value: 4.	W
RX_WIN	16	28, 29	Window for receive slot. The 2 LSBs are always zero. Minimum value: 4.	W
TX_START	14	30, 31	The start of the transmit slot. Default value: 0x3FFF.	W
TX_DEL	9	32, 33	Delay for powering up and calibration of analog sections (size will depend on the HW delay). This corresponds to the delay between TX_START and the 1st bit out of the Tx buffer. The 2 LSBs are always zero. Minimum value: 4.	W
TX_WIN	10	34, 35	Window for transmit slot. The 2 LSBs are always zero. Minimum value: 4.	W
MON_START0	14	36, 37	The start of the monitor 0 slot. RX_DEL controls the delay of the monitor slot. Default value: 0x3FFF.	W
MON_START1	14	38, 39	The start of the monitor 1 slot. RX_DEL controls the delay of the monitor slot. Default value: 0x3FFF.	W
MON_WIN	16	40, 41	Window for monitor slot. The 2 LSBs are always zero. Minimum value: 4.	W
INT_MASK_M	5	42, 43	Used to mask interrupts, global mask.	R/W
INT_PNDG_M	4	44, 45	Used to indicate the pending interrupts.	R
CNTRL_CODEC0	10	46, 47	Used to control the audio codec section. See the audio codec section.	W
CNTRL_CODEC1	11	48, 49	Used to control the audio codec section. See the audio codec section.	W
CNTRL_TONE	16	50, 51	High/low tones for DTMF/Ringer (8 bits each). See the audio codec section.	W
M_CONTROL2	16	52, 53	Control register accessed by the microcontroller. Usually the control bits in this register are more frequently accessed than the ones in the M_CONTROL1 register.	R/W
TX_OFFSET	16	54, 55	Tx offset correction, [7..0]: Tx I channel offset [15..8]: Tx Q channel offset	W
FREQL0	16	56, 57	Buffer register 0 for the lower 16 bits of the SYNDATA	W
FREQH0	16	58, 59	Buffer register 0 for the higher 16 bits of the SYNDATA	W
AGC0	10	60, 61	Buffer register 0 for the AUXDAC2	W
FREQL1	16	62, 63	Buffer register 1 for the lower 16 bits of the SYNDATA	W
FREQH1	16	64, 65	Buffer register 1 for the higher 16 bits of the SYNDATA	W
AGC1	10	66, 67	Buffer register 1 for the AUXDAC2	W
FREQL2	16	68, 69	Buffer register 2 for the lower 16 bits of the SYNDATA	W
FREQH2	16	70, 71	Buffer register 2 for the higher 16 bits of the SYNDATA	W

Table 5. AT75C6100 Register Map (Continued)

Name	Size	Addr	Function	R/W
AGC2	10	72, 73	Buffer register 2 for the AUXDAC2	W
SYNEN_CNTR0	14	74, 75	Register to hold the Q-bit count at which FREQ0 and AGC0 are transferred to the RF. Default value: 0x3FFF	W
SYNEN_CNTR1	14	76, 77	Register to hold the Q-bit count at which FREQ1 and AGC1 are transferred to the RF. Default value: 0x3FFF	W
SYNEN_CNTR2	14	78, 79	Register to hold the Q-bit count at which FREQ2 and AGC2 are transferred to the RF. Default value: 0x3FFF	W
PORT0_START	14	80, 81	Port 0 start count. Default value: 0x3FFF	W
PORT0_END	14	82, 83	Port 0 end count.	W
PORT1_START	14	84, 85	Port 1 start count. Default value: 0x3FFF	W
PORT1_END	14	86, 87	Port 1 end count.	W
PORT2_START	14	88, 89	Port 2 start count. Default value: 0x3FFF	W
PORT2_END	14	90, 91	Port 2 end count.	W
TX_FILDEL	6	92, 93	The total digital and analog filter delay in the transmitter path on the AT75C6100. Reserved for manufacturing purposes.	W
RX_FILDEL	7	94, 95	The digital delay in the receiver path on the AT75C6100. The 2 LSBs are always zero. Reserved for manufacturing purposes.	W
MODDEL	5	96, 97	Tx modulator delay. Reserved for manufacturing purposes.	R/W
WIN32	10	98, 99	Tx window for ramp_down. Reserved for manufacturing purposes.	R/W
PHASE_DEL	8	100, 101	bit[0..2]: 1/6.5 MHz delay steps bit[3]: reserved bit[4,5]: 1/1.083 MHz delay step. bit[6,7]: reserved. Reserved for manufacturing purposes.	W
DSP Data Space Mapped Registers				
Q_OFFSET	15	0	Used to adjust the Q-bit counter. Bit[14] indicates the mode of the adjustment.	W
RXIQ	16	1	Receive I/Q data FIFO	R
RXTX_GAIN	16	2	RX I and Q input gain: bit[2..0] = 001 = 0 dB 010 = 6 dB 100 = 12 dB, TX I and Q output gain: bit[10..8] = 001 = 0.5 V_{PP} output 010 = 1.0 V_{PP} output 100 = 1.5 V_{PP} output Unused bits are reserved.	W
TX_DATA	16	3	Transmit data FIFO	W
D_CONTROL	8	4	Control register accessed by the DSP	R/W

Table 5. AT75C6100 Register Map (Continued)

Name	Size	Addr	Function	R/W
INT_MASK_D	6	5	Used to mask interrupts, global mask.	R/W
INT_PNDG_D	5	6	Used to indicate the pending interrupts	R
AUDIO_IN	16	7	Receive audio sample	R
AUDIO_OUT	16	8	Send audio sample	W
AUXDAC1	10	9	Used for the AFC (also accessible by Micro)	W
AUXDAC2	10	10	Used for the AGC (also accessible by Micro)	W

Table 6. SYNCTRL0 Register Description

Bit	Name	Description
[4:0]	LOWVAL	This is the bit period at the start of which the selected LE signal(s) will be driven low. Bit periods on Syn_data are sequentially designated 0,1,...31, regardless of MSB/LSB selection. The allowed range for LOWVAL is [1..31]. A value of 0 disables the comparator.
[9:5]	HIGHVAL	This is the bit period at the start of which the selected LE signal(s) will be driven high. Bit periods on Syn_data are sequentially designated 0,1,...31, regardless of MSB/LSB selection. The allowed range for HIGHVAL is [0..30]. A value of 31 disables the comparator.
[12:10]	SEL[2..0]	Selects which synthesizer strobe line will be active. A “1” in any of these bits activates the corresponding latch enable.
[15:13]	reserved	

Table 7. SYNCTRL1 Register Description

Bit	Name	Description
[4:0]	NUMCLKS	This field defines the total number of clock pulses which are to be produced on the Syn_clk output. The value written into this field is the desired number of output clock pulses. If 32 clock pulses are desired, a zero is written into NUMCLKS. The design allows only up to 30 data bits to be transferred correctly.
[6:5]	CLKDIV	Selects rate for Syn_clk: 00 = MCLK/64, 01 = MCLK/32, 10 = MCLK/8, 11 = MCLK/2.
[7]	CLKPOL	Polarity of the Syn_clk. When CLKPOL = 1, the Syn_clk signal will have a rising edge in the middle of the data period with a 50% duty cycle pulse. CLKPOL = 0 reverses the polarity of Syn_clk.
[8]	MSBFRST	Writing a 0 to this bit causes the LSB (SYNDATA0[0]) to be the first bit sent to the Syn_data pin of the Synthesizer Serial Interface. Writing a “1” to this bit programs the block for MSB first operation (SYNDATA1[15]).
[9]	CLKDIS	Stops the generation of the Syn_clk
[15:10]	reserved	

Table 8. M_CONTROL1 Register Description

Bit	Name	Description	Default
[0]	SYNOL (Read)	Synthesizer out of lock. This is a Read only bit and when high, it indicates that one of the synthesizers is out of lock.	x
[1]	SYSRST	System reset. When set to high, this bit resets the AT75C6100 to its default initial state. The default value is 1 during reset and 0 after reset.	1 -> 0
[2]	CLKO1E	Output clock enable. When set to high, the CLKO1 pin outputs the 13 MHz clock.	0
[3]	DCLK	When high, the 520 kHz data clock to the DSP is active.	0
[4]	BBC_ON	When high, the Clk_in (master clock) is enabled. This signal is also ANDed with the BBCE pin input and both must be high for the AT75C6100 chip to receive the Clk_in.	0
[5]	RXRFOFF	The RX section of the RF subsystem is powered off if this bit is set. This is used only for emergency shut down. It is normally kept reset to zero.	0
[6]	TXRFOFF	The TX section of the RF subsystem is powered off if this bit is set. This is used only for emergency shut down. It is normally kept reset to zero.	0
[7]	INCLKDIV	Input clock divider. 0 : bypass divider (divide by 1) 1 : divide by 2	0
[8,9]	TXOFSTEN	Tx offset adjustment control: bit[9,8] = 00, no offset adjustment bit[9,8] = 01, enable internal digital calibration bit[9,8] = 10, enable external analog offset adjustment bit[9,8] = 11, not allowed.	00
[10]	TEOCALERR (Read only)	If set to 1, it indicates that the internal digital calibration is not completed.	0
[15:11]	reserved		

Table 9. M_CONTROL2 Register Description

Bit	Name	Description	Default
[1:0]	RXOFSTEN	00: disable dc offset corrections 01: enable internal digital correction 10: enable external analog correction 11: not allowed	00
[3:2]	TIMING_ADJ	This field adjusts the phase of the 13 MHz master clock by ±12/13 µs. 00: Normal (do not adjust), 01: Advance, 10: Retard, 11: not allowed	00
[4]	SYNEN	When set, this bit enables the synthesizer section to initiate a programming cycle. It is automatically disabled when a programming cycle ends. For scheduled programming mode, this bit is set by the control hardware.	0
[5]	SYNRDY (Read)	Synthesizer ready. This is a Read only bit and when high, it indicates that the synthesizer interface is idle and ready to be programmed.	x

Table 9. M_CONTROL2 Register Description (Continued)

Bit	Name	Description	Default
[10:6]	AUXCNTRL	Auxiliary DAC and ADC control: 01110: All auxiliary converters off xxxx1: DAC1 on xxx0x: DAC2 on xx0xx: DAC3 on x0xxx: DAC4 on 1xxxx: ADC on	01110
[11]	ADCRDY (Read)	Indicates that a data conversion by the ADC is ready.	x
[12]	OCTDEL	Introduces an octal bit delay to the transmitter timing: 0: no delay (normal mode) 1: octal bit period delay	0
[13]	DAC1IN	Selects the input to the DAC1: 0 = Microcontroller mapped 1 = DSP mapped	0
[14]	DAC2IN	Selects the input to the DAC2: 0 = Microcontroller mapped 1 = DSP mapped	0
[15]	REOCALERR (Read only)	If set to 1, it indicates that the analog external calibration is not completed.	0

Table 10. INT_MASK_M Register Description

Bit	Name	Description	Default
[0]	FRINT	Frame interrupt mask. When set high, the FR_int interrupt is enabled and an interrupt signal is generated. Disabled when low.	0
[1]	RXEND	Rx end of slot interrupt mask. When set high, the RX_end_int interrupt is enabled and an interrupt signal is generated. Disabled when low.	0
[2]	TXEND	TX end of slot interrupt mask. When set high, the TX_end_int interrupt is enabled and an interrupt signal is generated. Disabled when low.	0
[3]	MONEND	Monitor end of slot interrupt mask. When set high, the MON_end_int interrupt is enabled and an interrupt signal is generated. Disabled when low.	0
[4]	GINTDIS	Global interrupt disable. When set high, all interrupts to the microcontroller are disabled regardless of the individual interrupt mask bits.	0
[15:5]	reserved		

Table 11. INT_PNDG_M Register Description

Bit	Name	Description
[0]	FRINT	Frame interrupt pending. When high, it indicates that a FR_int is pending.
[1]	RXEND	Rx end of slot interrupt pending. When high, it indicates that an RX_end_int is pending.
[2]	TXEND	Tx end of slot interrupt pending. When high, it indicates that an TX_end_int is pending.
[3]	MONEND	Monitor end of slot interrupt pending. When high, it indicates that an MON_end_int is pending.
[15:4]	reserved	

Table 12. D_CONTROL Register Description

Bit	Name	Description	Default
[0]	RXFULL (Read)	Receive buffer 1st half ready to be read. This is a Read only bit. The bit is cleared (low) when second half of the buffer is full.	0
[1]	RXBUFRST	Receive buffer reset. When set high, the buffer pointers are reset to zero. This bit is reset automatically at the completion of the reset operation. (Read as 0)	0
[2]	TXBUFRST	Transmit buffer reset. When set high, the buffer pointers are reset to zero. This bit is reset automatically at the completion of the reset operation. (Read as 0)	0
[3]	RXCONT	Receive continuously. When this bit is set high, the receive counters are disabled and the AT75C6100 is put in a continuous receive mode. This mode is useful for testing purposes.	0
[4]	TXCONT	Transmit continuously. When this bit is set high, the transmitter counters are disabled and the AT75C6100 is put in a continuous transmit mode. This mode is useful for testing purposes.	0
[5]	RXEN	Receive enable. When this bit is reset to low, only the RX_start_int interrupt is generated. The AT75C6100 receive section and counters are powered down.	0
[6]	TXEN	Transmit enable. When this bit is reset to low, only the TX_start_int interrupt is generated. The AT75C6100 transmit section and counters are powered down.	0
[7]	MONEN	Monitor enable. When this bit is reset to low, only the MON_start_int interrupt is generated. The AT75C6100 receive section and counters are powered down.	0
[15:8]	reserved		

Table 13. INT_MASK_D Register Description

Bit	Name	Description	Default
[0]	RXSTART	Rx start interrupt mask. When set high, the RX_start_int interrupt is enabled and an interrupt signal is generated. Disabled when low.	0
[1]	TXSTART	Tx start interrupt mask. When set high, the TX_start_int interrupt is enabled and an interrupt signal is generated. Disabled when low.	0
[2]	MONSTART	Monitor start interrupt mask. When set high, the MON_start_int interrupt is enabled and an interrupt signal is generated. Disabled when low.	0
[3]	RXFIFO	Rx FIFO buffer interrupt mask. When set high, the RX_FIFO_int interrupt is enabled and an interrupt signal is generated. Disabled when low.	0
[4]	AUDIO	Audio interrupt mask. When set high, the Audio_int interrupt is enabled and an interrupt signal is generated. Disabled when low.	0
[5]	GINTDIS	Global interrupt disable. When set high, all interrupts to the DSP are disabled regardless of the individual interrupt mask bits.	0
[15:6]	reserved		

Table 14. INT_PNDG_D Register Description

Bit	Name	Description
[0]	RXSTART	Rx start interrupt pending. When high it indicates that an RX_start_int is pending.
[1]	TXSTART	Tx start interrupt pending. When high it indicates that a TX_start_int is pending.
[2]	MONSTART	Monitor start interrupt pending. When high it indicates that a MON_start_int is pending.
[3]	RXFIFO	Rx FIFO interrupt pending. When high it indicates that the Rx buffer has 16 pairs of new samples pending.
[4]	AUDIO	Audio interrupt pending. When high, it indicates that a new audio sample is available to be read and a new sample is requested for transmission.
[15:5]	reserved	

Table 15. CNTRL_CODEC0 Register Description

Bit	Name	Description	Default
[1:0]	FUNCSEL	Function select: 00: Power off to all codec sections x1: Audio section on 11: Tone generator on	00
[2]	TONESEL	Dual tone or single tone selection. When high, dual tone generation is activated.	0
[3]	AUXIN	Auxiliary input select. When high, the auxiliary input is selected.	0
[4]	AUXOUT	Auxiliary output select. When high, the auxiliary output is selected.	0
[5]	HPIN	Input (A/D) highpass filter select. When high, the input highpass filter is enabled.	0
[6]	HPOUT	Output (D/A) highpass filter select. When high, the output highpass filter is selected	0
[8, 7]	LPBCK	Loopback control. bit[8,7] = 00, no loopback bit[8,7] = 01, analog loopback (anti-aliasing output to power amp input) bit[8,7] = 10, decimator output to interpolator input (test 2). bit[8,7] = 11, digital audio output to digital audio input, (test 1)	00
[9]	DITHON	Dither enable bit. When high, dithering function is enabled.	0
[15..10]	reserved		

Table 16. CNTRL_CODEC1 Register Description

Bit	Name	Description	Default
[3..0]	OUTGAIN	Output gain. This controls the volume of the output signal. It controls the gain for both the audio and tone sections in steps of 2 dB. 0000: reserved 0001: 8 dB gain 0010: 6 dB gain ... 1111: -20 dB gain	1111
[4]	OUTMUTE	Output mute. When high, the output (spk) is muted.	1
[9:5]	INGAIN	Input gain. This controls the input PGA to the audio codec section. The gain is controlled in steps of 2 dB on a range of 0 to 48 dB. 00000: 0 dB gain 00001: 2 dB gain ... 01010: 20 dB gain ... 11000: 48 dB gain 11001 - 11111 reserved	00000
[10]	INMUTE	Input mute. When high, the input (mic/aux) is muted.	1
[15..11]	reserved		

Table 17. CNTRL_TONE Register Description

Bit	Name	Description
[7:0]	LOWTONE	Low tone frequency. Used for the lower tone of the DTMF or for the single tone frequency.
[15:8]	HIGHTONE	High tone frequency. Used for the high tone of the DTMF. Disabled when single tone mode is selected.

Radio Interface Electrical Characteristics

V_{DD} = 2.7V to 3.6V, t_{AMB} = -40°C to +85°C, worst case of process unless otherwise noted

Receive Side

Figure 4. Receive Path Block Diagram

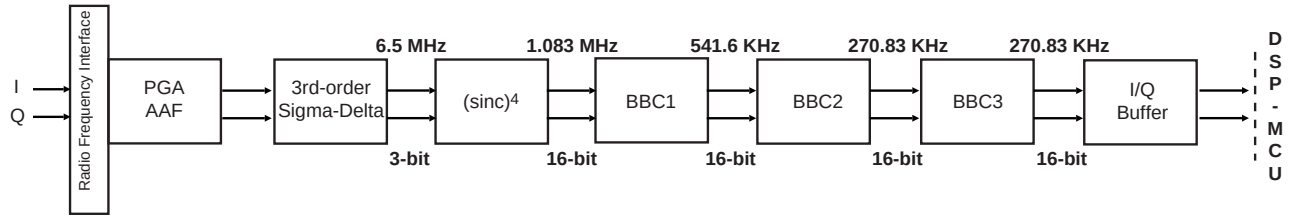


Figure 5. Magnitude Response of the Cascade of AAF, SINCF and Linear Phase FIR Filters BBC1, BBC2 and BBC3

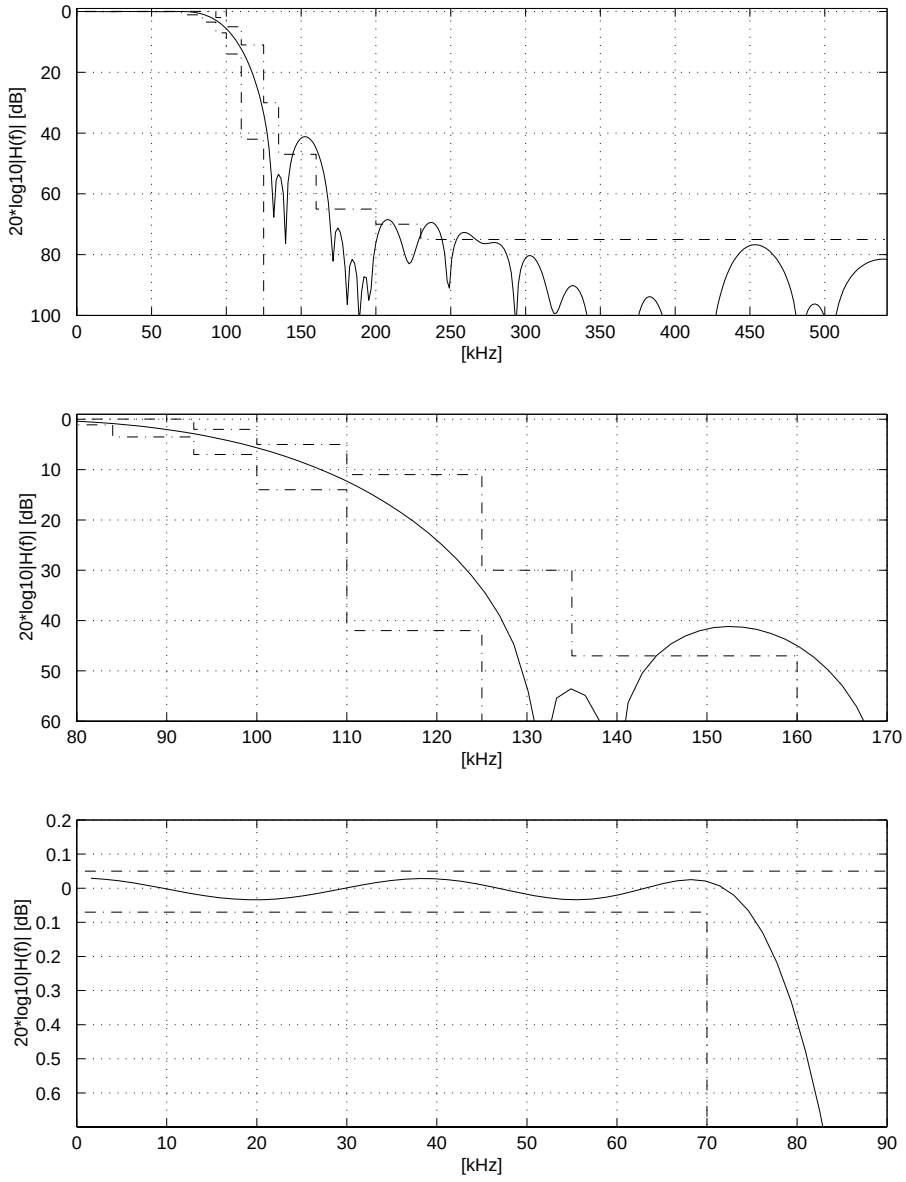


Table 18. AT75C6100 Electrical Characteristics - Receive Side

Parameter	Conditions	Min	Typ	Max	Unit
Output Resolution			16		bit
Sampling Frequency (A-to-D)			6.5		MHz
Output Sample Rate			270.83		kHz
Signal Bandwidth	-3 dB			96	kHz
Differential Input Level (peak to peak) for Full Scale Output	RINLEV[2:0] = [1 0 0] RINLEV[2:0] = [0 1 0] RINLEV[2:0] = [0 0 1]		1 2 4		V V V
PGA Gain Steps			6		dB
Input Resistance		50			kΩ
Dynamic Range	Extrapolated from -20 dBFS	80			dB
Image Rejection					
@ 6.5 MHz ± 100 kHz		102	120	134	dB
@ 13 MHz ± 100 kHz		88	109	119	
Offset Correction Range		-150		150	mV
Residual Offset after Calibration and Auto-zero		-1.22[(1)]		1.22 [(1)]	mV
Calibration Time	Calibration Clock @ 270.83 kHz		44.3		µs
Gain Matching between I and Q Channels		-0.11		0.11	dB
Max. Group Delay Deviation from Constant (0 to 96 kHz)		6.3	20	50	ns
Max. Group Delay between I and Q Channels (0 to 96 kHz)		7.4	12	17.5	ns
Power-on Settling Time				5	µs

1. $\pm V_{REF}/1024$; $V_{REF} = 1.25V$

Transmit Side

Figure 6. Transmit Path Block Diagram

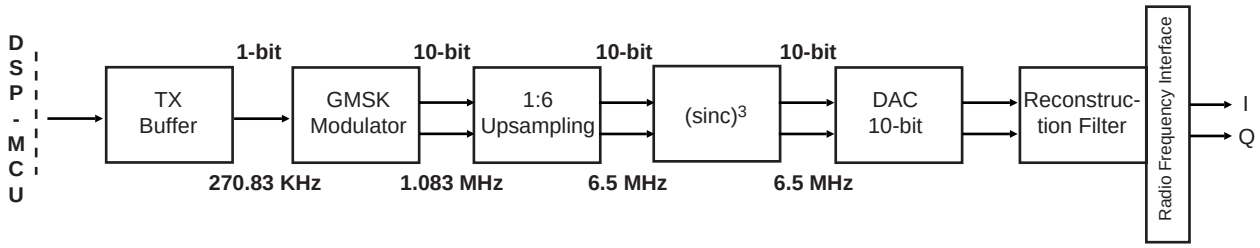


Figure 7. Magnitude Response of the AT75C6100 Transmit Path Including: Sinc Filter, DAC and Reconstruction Filter

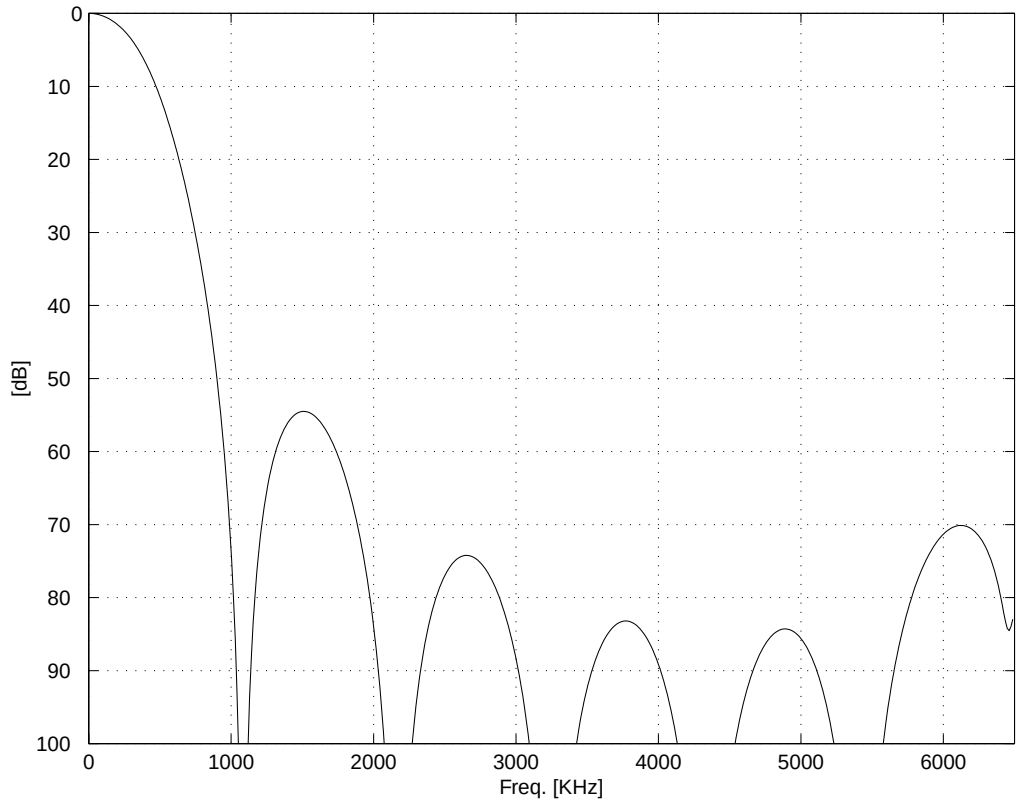


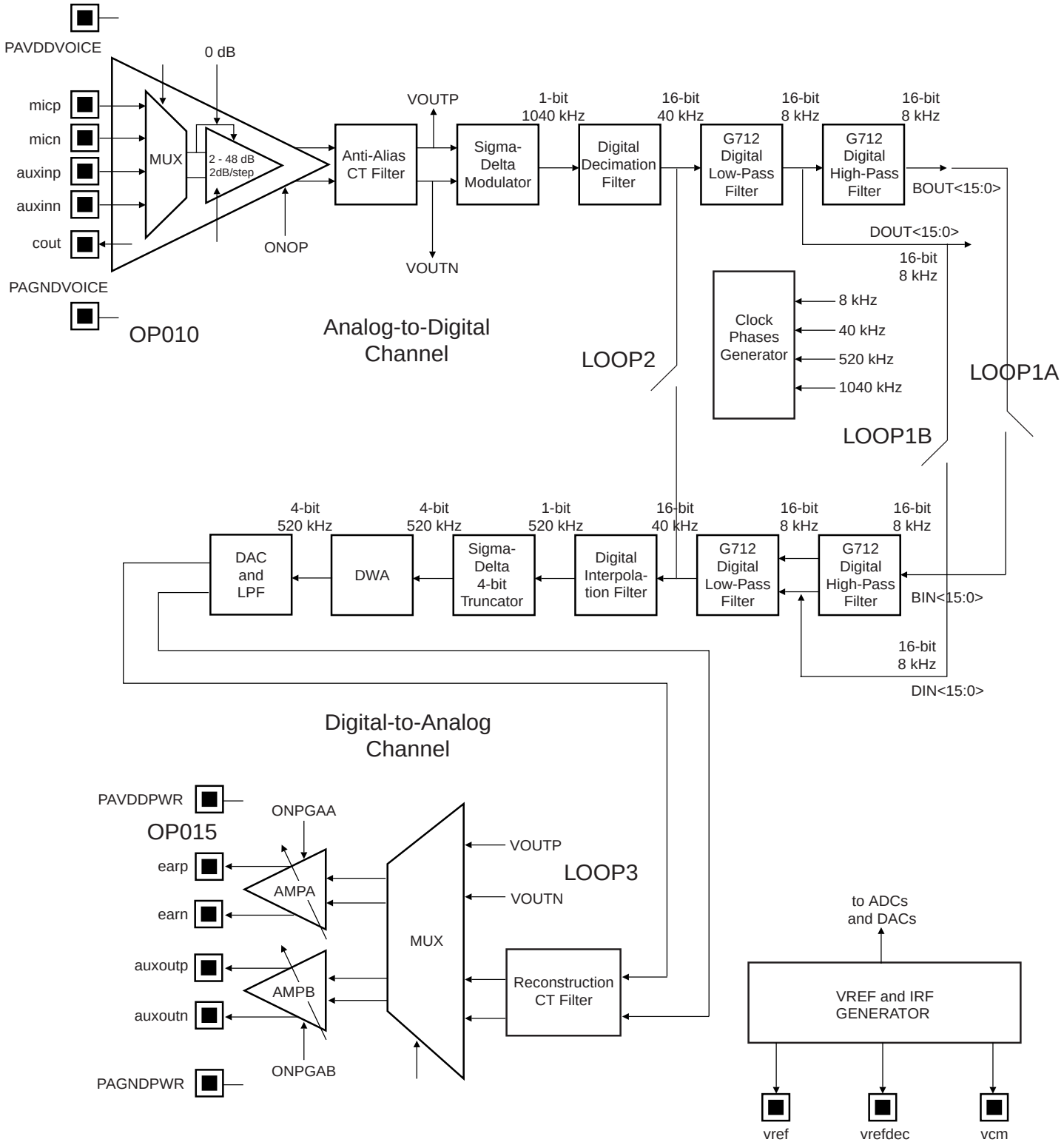
Table 19. AT75C6100 Electrical Characteristics - Transmit Side

Parameter	Conditions	Min	Typ	Max	Unit
DAC Resolution			10		bit
Input Bit Rate			270.83		kHz
Signal Bandwidth				100	kHz
Differential Output Swing (peak-to-peak)	TOUTLEV[2:0] = [1 0 0] TOUTLEV[2:0] = [0 1 0] TOUTLEV[2:0] = [0 0 1]		0.5 1.0 1.5		V V V
Output Load		5			kΩ
				100	pF
External Offset Adjustment Range		-150		150	mV
Internal Offset after Calibration (1)		-2		2	mV
I to Q Offset		-10		10	mV
Calibration Time				273.3	µs
Image Rejection					
@ 6.5 MHz ± 100 kHz		87	104	108	dB
@ 13 MHz ± 100 kHz		113	105	112	
Gain Matching between I and Q Channels		-0.1		0.1	dB
Max. Group Delay Deviation from Constant (0 to 96 kHz)		1.4	9	31	ns
Max. Group Delay between I and Q Channels (0 to 96 kHz)		7.7	14	22	ns
Power-On Settling Time				5	µs

1. (txin - txip) or (txqn - txqp) for digital data on each I and Q channel set to 1/2 full scale.

Voice Codec Functional Description

Figure 8. Voice Codec Block Diagram



Analog-to-Digital Channel

Analog Input Preamplifier

The analog input preamplifier is a two-multiplexed input programmable gain (2 to 48 dB, 2 dB step, 4-bit selection mode) microphone amplifier with automatic offset compensation.

The gain can be bypassed (0 dB) and at the same time save 200 µA of current.

The two differential input ports must be coupled to the external microphone.

Single-ended operation is possible if micn and auxinn are decoupled via a 100 nF capacitor to ground.

Offset compensation is achieved through a 100 nF capacitor connected between cout and ground.

Active Anti-alias Noise Filter

The anti-aliasing filter is based on a continuous-time, second-order, fully differential Rauch architecture. This filter provides 0.2 dB max gain flatness in the voice band, 50 kHz cutoff frequency, -55 dB attenuation at the A/D sampling frequency and -70 dB total harmonic distortion. The filter also functions as a buffer to the sigma-delta modulator. The circuit is internally biased by the on-chip voltage reference and its current consumption is less than 200 µA.

Analog-to-Digital Converter

The analog-to-digital converter consists of a second-order switched-cap sigma-delta modulator, based on a completely fully-differential SC architecture. Oversampling ratio is 130 and the clock frequency must be 1040 kHz.

Digital Filtering

Digital filtering is done in three stages. First, a $sinc^3$ decimator with decimation factor of 26 increases the output format to 16-bit word length while decreasing the sampling rate to 40 kHz.

Secondly, a digital low-pass filter, equivalent or superior to the CCITT G.712 recommendation, provides a strong rejection of out-of-band noise. The output data rate is decreased to the sampling rate of 8 kHz.

From there the 16-bit data are available for further processing, or can go through a high-pass filter which rejects the 100 Hz signals with a constantly flat response around 200 Hz. It is also effective in cancelling residual offset in the digital chain.

Digital-to-Analog Channel

Digital Filtering

As for the analog-to-digital channnel, a high-pass digital filter rejects the 100 Hz signals with a constantly flat response around 200 Hz with input and output sampling rate at 8 kHz. This filter can be bypassed and go directly to a low-pass image rejection filter equivalent or superior to the CCITT G.712 recomendation, which at the same time interpolates up to 40 kHz.

Then, a digital interpolator, with an interpolation factor of 13, raises the word rate up to 520 kHz.

Digital Sigma-Delta

A second-order multibit (n = 4) digital truncator is used to perform the noise shaping of the digital signal. Output format becomes 4-bit, 520 kHz sampling rate.

4-Bit Digital-to-Analog Converter

A multibit (n = 4) charge redistribution architecture is used to perform the digital-to-analog conversion. The multibit quantization preserves good SNR still with high amplitude signals approaching overload. The SC DAC is linearized with the DWA (data-weighted-averaging) dynamic element matching technique.

SC Low-pass Filter

An SC low-pass filter introduces a pole at 20 kHz to filter out the high-frequency components of the signal.

2nd-order Continuous Time Low-pass Filter

A continuous-time, second-order, fully-differential Rauch architecture is used for the reconstruction filter. The filter provides 0.2 dB max gain flatness in the voice band, 50 kHz cutoff frequency, and -70 dB total harmonic distortion. It also functions as a buffer for the power amplifiers. The circuit is internally biased by the on-chip voltage reference and its current consumption is less than 200 µA.

Output Multiplexer

An output multiplexer is provided in order to select the output of the digital-to-analog channel or the output of the analog-to-digital channel preamplifier (for test mode) and direct the selection either to a 32Ω earphone differential driver or to a 5kΩ/50 pF auxiliary differential driver. Both of the drivers have a power-down function capable of turning off unused power. At the same time, the load is disconnected.

Programmable Gain Attenuator

A programmable gain attenuator is placed before each of the differential output amplifiers to adjust the output signal level.

Gain programmability range is from +8 dB to -20 dB in steps of 2 dB. The last step of the attenuation is a MUTE function.

Voltage/Current References

Temperature- and power supply-independent voltage references (bandgap reference) are internally generated to provide stable biasing of all analog blocks. An internal voltage generator provides the analog virtual ground to all fully-differential analog blocks, and reference voltages to the sigma-delta analog-to-digital and digital-to-analog converters.

Only a 3.0V single power supply is required to operate the full system.

A decoupling capacitor in the order of 10 uF is necessary from VCM to ground. VREF and VREFDEC must be decoupled to ground with 100 nF.

Figure 9. Audio Codec Loopback Modes

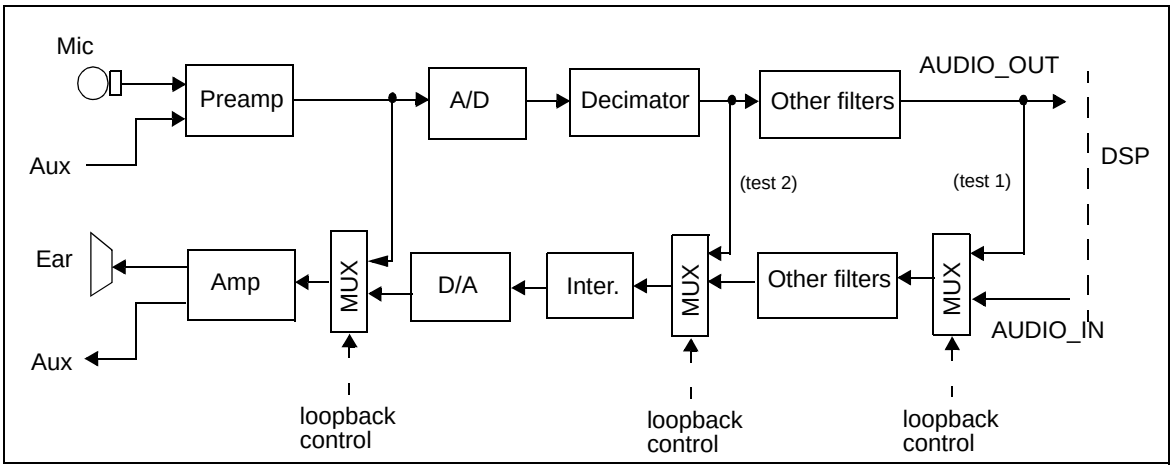
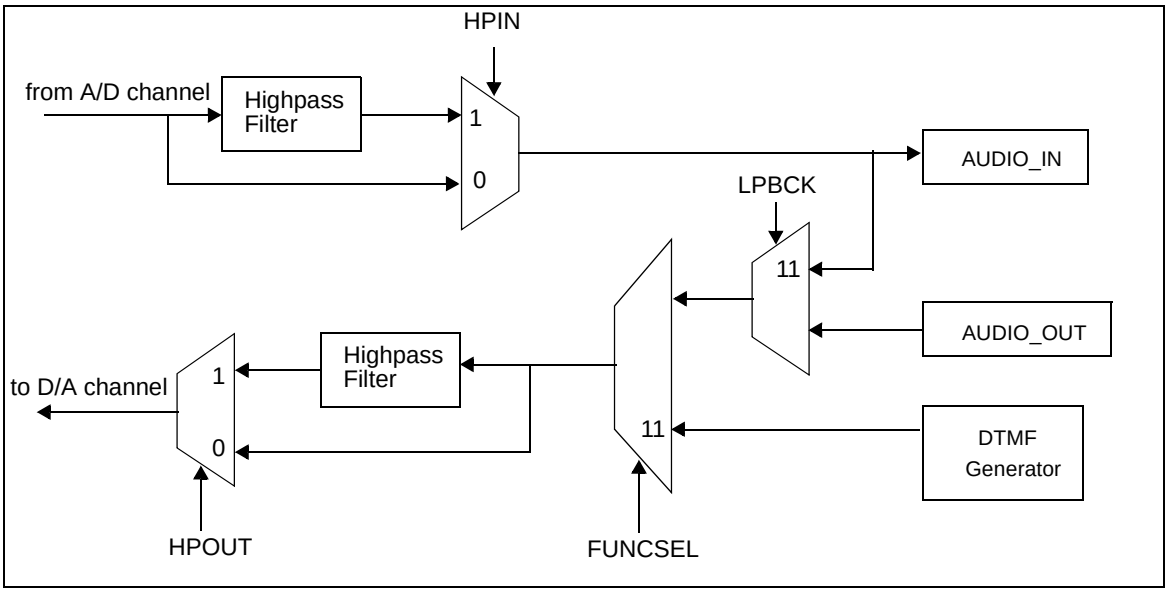


Figure 10. Audio Codec In/Out Muxes



Voice Codec Electrical Characteristics

V_{DD} = 2.7V to 3.6V, t_{AMB} = -40°C to +85°C, worst case of process unless otherwise noted

Table 20. Analog-to-Digital Channel

Parameter	Conditions	Min	Typ	Max	Unit
Preamp Input Offset Voltage	cout =100 nF	-10		10	mV
Gain Programmability	Steps of 2 dB	2		48	dB
Step Error		-0.5		0.5	dB
Input Impedance		100			kΩ
Startup Time	cout =100 nF		20		ms
0dBm0 Input Reference Level	Preamp gain = 0 dB/differential		1.700		V_{PP}
Maximum Input Level for Full Scale	Preamp gain = 0 dB/differential		2.448		V_{PP}
Absolute Gain Error	Preamp gain = 0 dB, 0 dBm0, 1020 Hz	-1		1	dB
Gain Tracking	ref@ -10 dB 3 dBm0 to -50 dBm0 -50 dBm0 to -60 dBm0	 -0.5 -1.5		 0.5 1.5	 dB dB
Gain Variation	V_{DD} and Temp	-0.5		0.5	dB
Signal-to-Distortion Ratio	Preamp gain = 0 dB, 0 dBm0, 300 to 3400 Hz		65	-60	dB
Intermodulation Distortion	Preamp gain = 0 dB, 0 dBm0, 300 to 3400 Hz			-60	dB
Frequency Response	Bit[5] of CNTRL_CODEC = 1 preamp gain = 0 dB, 0 dBm0 f = 0 to 150 Hz f = 150 to 170 Hz f = 170 to 200 Hz f = 200 to 3600 Hz f = 3600 to 3700 Hz f = 4000 Hz f > 4600 Hz	 -3 -0.25 -0.5		 -15 -3 -0.25 0.25 -0.25 -60 -60	 dB dB dB dB dB dB dB
Idle Channel Noise	Input shorted to Gnd		-74	-64	dBm0p
Crosstalk	Preamp gain = 0 dB, 0 dBm0, 1020 Hz Measured on DAC with idle code			-65	dB
Power Supply Rejection Ratio	Input grounded, 100 mV_{PP} @1020 Hz on AVDD and DVDD		-55		dB
Absolute Group Delay				360	µs
Group Delay Distortion	Ref to absolute group delay f = 500 Hz f = 600 Hz f =1000 Hz f = 2600 Hz f = 2800 Hz			 750 380 130 130 750	 µs µs µs µs µs
Coding	2’s complement				

Table 21. Digital-to-Analog Channel - Measured on 600Ω between earp and earn unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Unit
(Main) Power AMP with Volume Control					
Output Voltage Range	V_{DD} = 3V, differential between earp and earn, 150Ω load			3.2	V_{PP}
Output Voltage Range	V_{DD} = 3V, differential between earp and earn, 32Ω load			1.5	V_{PP}
Output Offset Voltage	Single-ended	-80		80	mV
Output Offset Voltage	Differential	-20		20	mV
Maximum Output Current	Differential	-45		45	mA
Output Load	Differential	32	150		Ω
Total Harmonic Distortion	Differential/ 150Ω, 100 nF	-40	-46		dB
Volume Control Range		-20		+8	dB
Volume Control Step Size		-0.5	3	0.5	dB
Signal Attenuation	Mute	-60			dB
Aux AMP with Volume Control					
Output Voltage Range	V_{DD} = 3V, differential, 5 kΩ			3.2	V_{PP}
Output Offset Voltage	Single-ended	-80		80	mV
Output Offset Voltage	Differential	-20		20	mV
Minimum Output Load	Differential	5	10		KΩ
Total Harmonic Distortion	Differential/5 kΩ/50 pF	-50			dB
Volume Control Range		-20		+8	dB
Volume Control Step Size		-0.5	3	0.5	dB
Signal Attenuation	Mute	-60			dB
0 dBm0 Input Reference Level	Amp gain = 0 dB/differential		1.4		V_{PP}
Full Scale Output Level	Amp gain = 0 dB/differential		2.016		V_{PP}
Absolute Gain Error	Amp gain = 0 dB/differential, 1020 Hz 0 dBm0	-1		1	dB
Gain Tracking	Ref@ -10 dB 3dBm0 to -50dBm0 -50dBm0 to -60dBm0	 -0.5 -1.5		 0.5 1.5	 dB dB
Gain Variation	V_{DD} and Temp	-0.5		0.5	dB
Signal-to-Distortion Ratio	Gain = 0 dB, 0dBm0, 300 to 3400 Hz, 600Ω load on Power amp (differential)			-48	dB
Intermodulation Distortion	Gain = 0 dB, 0dBm0, 300 to 3400 Hz, 600Ω load on Power amp (differential)			-60	dB

Table 21. Digital-to-Analog Channel - Measured on 600Ω between earp and earn unless otherwise specified (Continued)

Parameter	Conditions	Min	Typ	Max	Unit
Frequency Response	Gain = 0 dB, 0dBm0 f = 0 to 150 Hz f = 150 to 170 Hz f = 170 to 200 Hz f = 200 to 3600 Hz f = 3600 to 3700 Hz f = 4000 to 100 kHz	 -3 -0.25 -0.5 	 	 -15 -3 -0.25 0.25 -0.25 -60	 dB dB dB dB dB dB
Idle Channel Noise	Idle Code		-70	-57	dBm0p
Crosstalk	Preamp gain = 0 dB, 0dBm0, 1020 Hz Measured on ADC with input shorted			-65	dB
Power Supply Rejection Ratio	Input grounded, 100 mV_{PP} @1020 Hz on AV_{DD} and DV_{DD}		-55		dB
Absolute Group Delay				240	µs
Group Delay Distortion	Ref to absolute group delay f = 500 Hz f = 600 Hz f = 1000 Hz f = 2600 Hz f = 2800 Hz	 	 	 750 380 130 130 750	 µs µs µs µs µs

Auxiliary Functions

The AT75C6100 contains the necessary data converters to enable communication between the DSP and the RF subsystem. Additional peripherals, e.g. a battery pack, can also be accessed through the AT75C6100.

Digital-to-Analog Converters

The AT75C6100 contains 4 digital-to-analog data converters (DAC). Three of these DACs are used by AGC, AFC and Tx Power signals. The fourth DAC is reserved for auxiliary functions, e.g. an LCD.

Each of the DACs has a memory-mapped register which can be accessed by the microcontroller. DAC1 (AFC) and DAC2 (AGC) are also accessible by the DSP. To minimize power consumption, the AGC and Tx Power DACs should be powered up only during the slots they are needed. The AFC DAC gives the control signal to the VCTCXO and consequently needs to be on whenever the VCTCXO is on. The AUXCNTRL field in the M_CONTROL2 register controls the powering up and down of the DACs. For example the AGC is needed only during the receive operations and can be powered down during the transmit operation. When the DACs are powered down, although the data conversion stops, the registers holding the DAC values retain their contents. They are initialized to all zeroes during system reset.

In addition to the analog AGC signal, the 5 LSBs of the AUXDAC2 (AGC) are brought out of the AT75C6100 as 5 digital pins. The user can use these bits to control an RF with a digital AGC capability by programming the 5 LSBs of the AUXDAC2 register.

Table 22 shows the specifications for these converters.

Table 22. Digital-to-Analog Converter Specifications

Parameter	Conditions	Min	Typ	Max	Units
AFC DAC					
Full Scale Output Voltage			2.5		V
Resolution			10		bits
Gain and Offset Error		-3		3	%
Integral Non-linearity	Corresp. to max. error of 30 Hz, assuming the full DAC range is 30 kHz		0.5		LSB
Differential Non-linearity		-0.5		0.5	LSB
Conversion Rate	Settling time < 3 µs		270.83		kHz
Resistive Load		10			kΩ
Capacitive Load				50	pF
AGC and Tx Power DACs					
Full Scale Output Voltage			2.5		V
Resolution			10		bits
Gain and Offset Error		-3		3	%
Integral Non-linearity				4	LSB
Differential Non-linearity				1	LSB
Conversion Rate			270.83		kHz
Resistive Load		10			kΩ
Capacitive Load				50	pF
AUX DAC					
Full Scale Output Voltage			2.5		V
Resolution			8		bits
Gain and Offset Error		-5		5	%

Table 22. Digital-to-Analog Converter Specifications (Continued)

Parameter	Conditions	Min	Typ	Max	Units
Integral Non-linearity		-4		4	LSB
Differential Non-linearity				1	LSB
Conversion Rate			270.83		kHz
Resistive Load		10			kΩ
Capacitive Load				50	pF

Analog-to-Digital Converter

The AT75C6100 has one successive approximation type 10-bit analog-to-digital converter with three multiplexed input ports. The most common usage of the ADC is for battery voltage and temperature monitoring.

There are three distinct input pins, one for each port multiplexed internally to form one input to the ADC. The output of the ADC is demultiplexed into 3 ports, each accessing a memory-mapped register as shown in Figure 11. The mux and demux are synchronized to read in the input to the corresponding register. A conversion is initiated by the microcontroller writing into the desired memory mapped register. This action powers up the ADC and performs a new conversion. The conversion time is 45 µs. Upon settling, a status bit (ADCRDY) in the M_CONTROL2 register indicates the availability of a new data in the corresponding register. The ADCRDY bit should only be polled after a conversion has been initiated, otherwise it is invalid.

Table 23 shows the specifications for the ADC.

Figure 11. Analog-to-Digital Converter Multiplexing and Demultiplexing

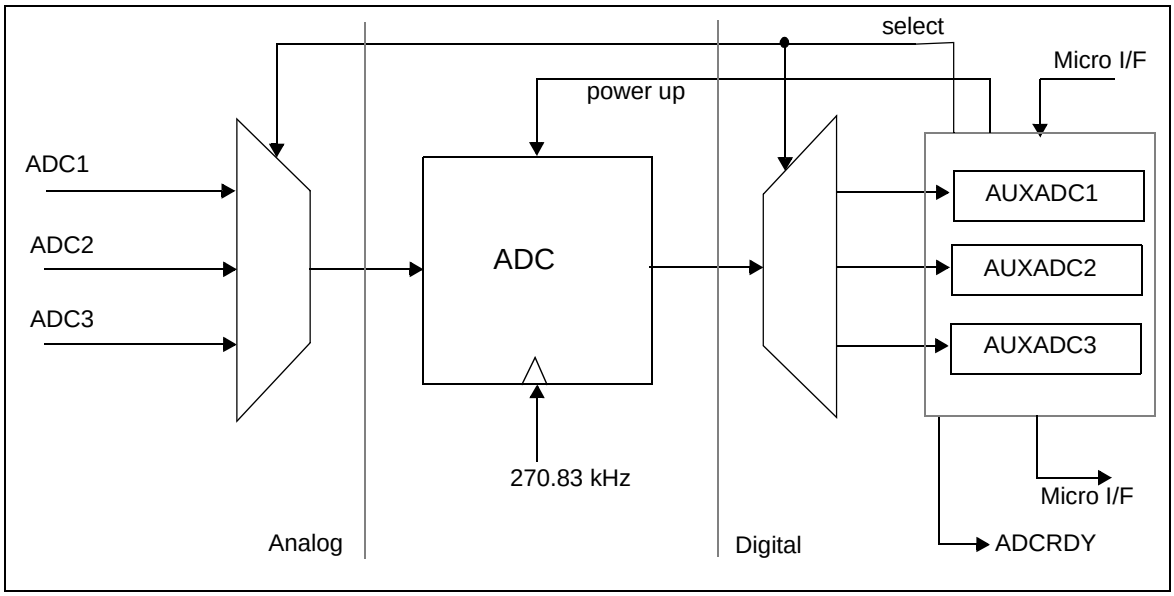


Table 23. Auxiliary Analog-to-Digital Converter Specifications

Parameter	Conditions	Min	Typ	Max	Units
Full Scale Input Voltage			2.5		V
Resolution			10		bits
Gain and Offset Error		-4		4	%
Integral Non-linearity				4	LSB
Differential Non-linearity				1	LSB
Conversion Time	Conversion time takes 12 clock cycles		44.3		µs
Number of Ports			3		
Input Resistive Impedance			100		kΩ
Clock Frequency			270.83		kHz

AT75C6100 Current Consumption

Table 24. AT75C6100 Current Consumption Figures

	100% Active	Standby Mode
Transmit Channel	9.4 mA	40 µA
Receive Channel	28.7 mA	150 µA
Aux ADC	65 µA	0.33 µA
Power DAC	290 µA	7 µA
AGC DAC	290 µA	7 µA
AFC DAC	370 µA	15 µA
Voltage References	1 mA	10 µA
	0.5 mA (Rx alone)	10 µA
Voice Codec	6 mA	63 µA
Digital Section	10.5 mA	10 µA

Figure 12. TQFP144 Package Drawing

Table 25. Common Dimensions (mm)

Symbol	Min	Nom	Max
c	0.09		0.2
c1	0.09		0.16
L	0.45	0.6	0.75
L1	1.00 REF		
R2	0.08		0.2
R1	0.08		
S	0.2		
q	0°	3.5°	7°
θ1	0°		
θ2	11°	12°	13°
θ3	11°	12°	13°
A			1.6
A1	0.05		0.15
A2	1.35	1.4	1.45
Tolerances of form and position			
aaa		0.2	
bbb		0.2	

Table 26. Lead Count Dimensions (mm)

Pin Count	D/E BSC	D1/E1 BSC	b			b1			e BSC	ccc	ddd
			Min	Nom	Max	Min	Nom	Max			
144	22.0	20.0	0.17	0.22	0.27	0.17	0.2	0.23	0.50	0.10	0.08

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